line voltage V_{word} **325** will be at a voltage approaching that of the power supply voltage source V_{cc}. The voltage of the bit-lines V_{bit} **320** will again also be precharged to a voltage that is one half the power supply voltage source $V_{cc}/2$.

The n-MOS transistor M1 **300** will be conducting and place the voltage V_c **605** of the storage capacitor C **305** at the base **420** of the pnp transistor Q1 **310**. The pnp transistor Q1 **310** will be conducting the current I_{bit} **600** at the maximum available current level I_{max}. This level of the bit-lines current I_{bit} will interpreted by the sense amplifier as the logical "0"

Refer now to FIGS. **7***a,* **7***b,* **7***c,* and **7***d* to understand the write operation of the DRAM cell. FIG. **7***a* shows the writing of a logical "1" to the DRAM cell. The voltage of the word line V_{word} **325** will be set to the power supply voltage source V_{cc} to activate the n-MOS transistor M1 **300** to conduct. The voltage of the bit-lines V_{bit} **320** will be set to the level of the power supply voltage source V_{cc}. If the storage capacitor C **305** has been discharged to a level approaching 0 V, p/n junction of the emitter-base junction of the pnp transistor Q1 **310** will be forward biased to charge the storage capacitor C **305** to the level approaching the power supply voltage source V_{cc}. If, however, the storage capacitor C **305** is already charged to the level of the power supply voltage source V_{cc}, there will be no response to the change.

The operation of reading a logical "1" and logical "0" and writing a "1" of the DRAM cell of this invention to this point is not different to that shown in the prior art. The writing of the logical "0" is different as described below.

Refer now to FIG. **7***b* to understand the writing of a logical "0" to the DRAM cell. The voltage of the word line V_{word} **325** is set to the power supply voltage source V_{cc} to activate the n-MOS transistor M1 **300**. The voltage of the bit-lines V_{bit} **320** is set to 0 V. As biased, the pnp transistor Q1 **310** will be in a nonconductive state. If the storage capacitor C **305** is discharged to a level V_c **605** that is 0 V, the cell will have already been set to a logical "0" and no response is necessary. If however, the storage capacitor C **305** is charged to a voltage V_c **605** that is approaching the voltage level of the power supply voltage source V_{cc}, the bipolar pnp transistor Q1 **310** will again be in a nonconductive state. To overcome the slow discharge of the storage capacitor C **305** due to leakage as in the prior art, a gate induced drain leakage (GIDL) current will cause the rapid discharge of the storage capacitor C **305**.

Refer now to FIGS. **7***c* and **7***d* to understand the GIDL effect. The overlaps OV1 **470** and OV2 **475** of the gate over the n-base **420** and the p^+ emitter **425** will allow electrons e^- to create a current at the surface of the p^+ emitter **425** to flow to the n-base **420** through the channel **465** to discharge the storage capacitor C **315**.

The field ϵ **710** created by the voltage at the word line V_{word} **325** will cause electrons to be generated at the interface of the p^+ emitter **425** by band-to-band tunneling . The gate oxide **440** must be thin enough so that the vertical field ϵ **710** is large enough (>2 Mev/cm) to trigger the band-to-band tunneling. This will cause and enhanced junction leakage current to flow across the reversed biased diode of the p^+ emitter **425** and the n-base **420**. Or as shown in FIG. **7***d,* the electrons e^-**750** are generated from the valence band E_v **755** through conduction band E_c **760** through the depletion layer **715** on the p^+ emitter **425** surface by band-to-band tunneling mechanism, they will flow in the n-base **420** and through the inverted channel **700** to the drain **435** of the n-MOS transistor M, **300** to discharge the storage capacitor C **305**.

As can be seen by those skilled in the art, the reversal of the material types to use p-MOS transistors and an npn transistor with appropriate changes in biasing voltages is in keeping with the structure and operation of this invention.

While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

The invention claimed is:

1. A DRAM cell fabricated within an array of DRAM cells upon a semiconductor substrate, comprising:

a) a charge storage capacitor to store an electrical charge representing a bit of digital data, having a first plate and a second plate coupled to a substrate biasing voltage source;

b) a MOS transistor having a gate coupled to a word line control to activate and deactivate said MOS transistor, a drain coupled to the first plate of said charge storage capacitor, and a source, whereby said gate is formed by:

depositing, masking and etching of an insulating material upon said semiconductor substrate to form a gate oxide in an area between said drain and said source, and

depositing masking and etching a conductive material such as polysilicon on said gate oxide to form said gate and;

c) a bipolar transistor to amplify the electrical charge stored on said charge storage capacitor, having

a base that functions as said source for said MOS transistor and is formed by the steps of:

placing a first implant mask and implanting a first material of the first conductivity type adjacent to said gate oxide to form said base, whereby said implanting has a high energy and a large angle,

a collector formed by a bulk material of said semiconductor substrate and coupled to a substrate biasing voltage source, and

an emitter coupled to a bit-lines control which when activated will sense the charge amplified by said bipolar transistor and formed by the steps of:

placing a second implant mask and implanting a second material of the second conductivity type within said first material of the first conductivity type and adjacent to said gate to form said emitter, whereby said implanting has a high dosage of said second material of the second conductivity type to ensure a large overlap of said gate of said emitter.

2. The DRAM cell of claim **1** whereby during forming of said bipolar transistors, the implanting to form said base has the high energy and the large angle to provide a large current gain.

3. The DRAM cell of claim **1** wherein during the forming of said bipolar transistor, the implanting to form the emitter has a high dosage of the second material of the second conductivity type to ensure a large overlap of said gate of said emitter.

4. The DRAM cell of claim **3** wherein said overlap of said gate of said emitter is to ensure generation of gate induced drain leakage current at a surface of said semiconductor wafer in the area of said overlap so as to provide a discharge of said storage capacitor during writing of a logical "0" to said storage capacitor.

5. The DRAM cell of claim **1** whereby during forming of said bipolar transistor, the implanting of the base is accomplished by implanting phosphorus P^{31} at a range of energy from approximately 50 Kev to approximately 100 Kev to a